WHAT IS CLAIMED IS:

1. A capacitance measurement circuit comprising:

first, second and third terminals, said first terminal being accompanied by a first capacitance including first and second capacitance components to be measured and a non-target capacitance component not to be measured, said third terminal being accompanied by a dummy capacitance having the same capacitance value as said non-target capacitance component;

a first current detector detecting a first current supplied to said first terminal;

a second current detector detecting a second current induced from said second terminal;

a third current detector detecting a third current supplied to said third terminal; and

a target capacitance forming section formed between said first terminal and said second terminal so that said first terminal is accompanied by said first capacitance component,

said target capacitance forming section, said first to third terminals, and said first to third current detectors constituting a capacitance measurement section.

2. The capacitance measurement circuit according to claim 1, wherein

said first to third current detectors include at least one transistor,

said at least one transistor including a transistor which has a transistor characteristic of being less apt to cause a leakage current than an ordinary transistor which constitutes a logic circuit.

3. The capacitance measurement circuit according to claim 1, wherein

said first to third current detectors include at least one transistor of a first conductivity type,

said at least one transistor being formed in a well region of a second conductivity type,

said well region being selectively formed in an upper layer of a bottom region of the first conductivity type.

4. The capacitance measurement circuit according to claim 1, wherein

said first to third current detectors include first and second transistors of different conductivity types,

said first and second transistors being formed in a semiconductor layer of an SOI substrate which is formed of a buried insulating layer and said semiconductor layer formed on said buried insulating layer,

said first and second transistors being isolated from each other by an element isolation region which extends to said buried insulating layer.

5. The capacitance measurement circuit according to claim 1, wherein

said capacitance measurement section includes first and second circuits,

said first and second circuits each comprising said first to third terminals and said first to third current detectors,

said first and second circuits respectively including, as said target capacitance forming section, first and second target capacitance forming sections which are different from each other,

said first capacitance component includes first and second partial capacitance

components,

said first target capacitance forming section substantially includes said first and second partial capacitance components, and

said second target capacitance forming section substantially includes only said second partial capacitance component.

6. The capacitance measurement circuit according to claim 5, wherein

said first and second target capacitance forming sections include first and second measurement transistors, respectively,

said first and second measurement transistors each having a gate electrode and a pair of electrode regions, said gate electrode being electrically connected to said second terminal, one of said pair of electrode regions being electrically connected to an interconnect layer which is electrically connected to said first terminal,

said first partial capacitance component includes a coupling capacitance formed between said contact hole and said gate electrode,

said second partial capacitance component includes a coupling capacitance formed between said gate electrode and said interconnect layer,

in said first measurement transistor, a distance from said gate electrode to said contact hole is set to a length with which said first partial capacitance component is effective, and

in said second measurement transistor, a distance from said gate electrode to said contact hole is set to a length with which said first partial capacitance component is ineffective.

7. The capacitance measurement circuit according to claim 5, wherein

said first and second target capacitance forming sections include first and second measurement transistors, respectively,

said first and second measurement transistors each having a gate electrode, and first and second electrode regions which are electrically connected through first and second contact holes to first and second interconnect layers which are electrically connected to said first and second terminals, respectively,

said first partial capacitance component includes a coupling capacitance formed between said first and second contact holes,

said second partial capacitance component includes a coupling capacitance formed between said first and second electrode regions,

in said first measurement transistor, said first and second contact holes are formed such that said first partial capacitance component is effective, and

in said second measurement transistor, at least one of said first and second contact holes is formed such that said first partial capacitance component is zero.

8. A capacitance measurement circuit comprising:

a first terminal accompanied by a first capacitance including first and second capacitance components, said first capacitance component including a predetermined number of first capacitance components;

a predetermined number of second terminals;

a first current detector detecting a first current supplied to said first terminal;

a second current detector detecting a second current obtained from a common signal line;

a target capacitance forming section formed between said first terminal and said predetermined number of second terminals so that said first terminal is accompanied by

said first capacitance component, said target capacitance forming section having said predetermined number of first capacitance components formed between said first terminal and said predetermined number of second terminals; and

a selector selecting one of said predetermined number of second terminals as a selected terminal in response to an external signal whose bit number is smaller than said predetermined number, and transmitting said second current induced from said selected terminal to said common signal line.

9. The capacitance measurement circuit according to claim 8, wherein

said selector includes:

a plurality of latches serially inputting one bit of said external signal; and

a terminal selector selecting one of said plurality of second terminals according to latch data in said plurality of latches.

10. A capacitance measurement circuit comprising:

first and second terminals;

a current detector detecting a supply current supplied to said first terminal;

a terminal state changer selecting either a first state in which said second terminal is connected to a fixed potential or a second state in which said first and second terminals are short-circuited; and

a target capacitance forming section formed between said first and second terminals and having a measuring target capacitance including first and second capacitance components,

said target capacitance forming section, said first and second terminals, said current detector, and said terminal state changer constituting a capacitance measurement

section.

11. The capacitance measurement circuit according to claim 10, wherein

said capacitance measurement section includes first and second circuits,

said first and second circuits each including said first and second terminals, said current detector and said terminal state changer,

said first and second circuits respectively including, as said target capacitance forming section, first and second target capacitance forming sections which are different from each other.

12. The capacitance measurement circuit according to claim 11, wherein

said measuring target capacitance includes a non-target capacitance component not to be measured, and

said first and second target capacitance forming sections are formed to be capable of removing said non-target capacitance component and measuring said first and second capacitance components on the basis of four values of said supply current which are obtained in said first and second states of said first and second circuits.

13. The capacitance measurement circuit according to claim 12, wherein

said measuring target capacitance includes a third capacitance component to be measured,

said first and second target capacitance forming sections are formed to be capable of removing said non-target capacitance component and measuring at least one of said first to third capacitance components on the basis of four values of said supply current which are obtained in said first and second states of said first and second circuits.

14. The capacitance measurement circuit according to claim 13, wherein

said first target capacitance forming section includes:

a first semiconductor substrate;

first and second electrodes electrically connected to said first and second terminals;

first and second active regions selectively formed in a predetermined region of a surface of said first semiconductor substrate, said first and second active regions being electrically connected to said first and second electrodes, respectively; and

an isolation region providing isolation between said first and second active regions,

said second target capacitance forming section includes:

a second semiconductor substrate equivalent to said first semiconductor substrate; and

an insulating region formed in a region which corresponds to at least said predetermined region of a surface of said second semiconductor substrate,

one of said first and second capacitance components includes a coupling capacitance formed between said first and second electrodes, and

said third capacitance component includes a coupling capacitance formed by said first and second active regions and said isolation region formed between said first and second active regions.

15. The capacitance measurement circuit according to claim 14, wherein

said first target capacitance forming section is characterized in that a dummy active region equivalent to said first and second active regions is formed in a region of the

surface of said first semiconductor substrate other than said predetermined region.

16. The capacitance measurement circuit according to claim 14, wherein

said first and second semiconductor substrates each include an SOI substrate having a buried insulating layer and a semiconductor layer formed on said buried insulating layer,

in said first target capacitance forming section, said first and second active regions are formed in a surface of said semiconductor layer, and

in said second target capacitance forming section, said insulating region is formed in the surface of said semiconductor layer.

17. The capacitance measurement circuit according to claim 16, wherein

said isolation region includes an isolation region which extends from the surface of said semiconductor layer to said buried insulating layer, and

said first and second active regions are completely isolated from each other by said buried insulating layer and said isolation region.

18. The capacitance measurement circuit according to claim 17, wherein

said first and second active regions include an active region which extends from the surface of said semiconductor layer to said buried insulating layer.

19. The capacitance measurement circuit according to claim 14, wherein

said first and second electrodes each have a comb-like structure having a plurality of teeth, said plurality of teeth of said first electrode and said plurality of teeth of said second electrode being located in opposed spaced relation with predetermined

intervals, and

said first and second active regions include a plurality of first and second active regions which are alternately formed with said isolation region sandwiched in between, said plurality of first and second active regions being electrically connected through contact holes to said plurality of teeth of said first and second electrodes, respectively.

20. The capacitance measurement circuit according to claim 13, wherein

said first and second target capacitance forming sections each include:

a semiconductor substrate;

first and second interconnect layers electrically connected to said first and second terminals, respectively;

first and second active regions selectively formed in a predetermined region of a surface of said semiconductor substrate, said first active region being electrically influenced by said first interconnect layer, said second active region being electrically connected to said second interconnect layer through a contact hole; and

an isolation region providing isolation between said first and second active regions,

said third capacitance component includes a coupling capacitance formed by said first and second active regions and said isolation region formed between said first and second active regions, and

said first and second target capacitance forming sections each employ said first active region having a different area size.

21. The capacitance measurement circuit according to claim 20, wherein

in said first and second target capacitance forming sections, said first active

region is electrically connected through a contact hole to said first interconnect layer.

22. The capacitance measurement circuit according to claim 20, wherein said first and second target capacitance forming sections each include:

a gate insulating film formed on said first active region;

a gate electrode formed on said gate insulating film; and

a contact hole providing electrical connection between said gate electrode and said first interconnect layer.

23. A capacitance measurement circuit comprising:

first and second terminals;

first and second pads;

a first current detector detecting a first current supplied to said first terminal;

a second current detector detecting a second current supplied to said second terminal; and

a ring load section electrically connected to said first terminal,

said ring load section including first and second inverters connected in series in the order named,

said first inverter including a first transistor of a first conductivity type, and a second transistor of a second conductivity type,

said first transistor having a first electrode, a second electrode and a control electrode, said first and control electrodes of said first transistor being electrically connected in common to said first pad,

said second transistor having a first electrode, a second electrode and a control electrode, said first and control electrodes of said second transistor being electrically

connected in common to said second pad, said control electrodes of said first and second transistors being electrically isolated from each other, said second electrodes of said first and second transistors being electrically connected in common to said first terminal.

24. A method of analyzing interconnect characteristics using a capacitance measurement circuit,

said capacitance measurement circuit comprising:

a first terminal accompanied by a first capacitance including first and second capacitance components, said first capacitance component including a predetermined number of first capacitance components;

a predetermined number of second terminals;

a first current detector detecting a first current supplied to said first terminal;

a second current detector detecting a second current obtained from a common signal line;

a target capacitance forming section formed between said first terminal and said predetermined number of second terminals so that said first terminal is accompanied by said first capacitance component, said target capacitance forming section having said predetermined number of first capacitance components formed between said first terminal and said predetermined number of second terminals; and

a selector selecting one of said predetermined number of second terminals as a selected terminal in response to an external signal whose bit number is smaller than said predetermined number, and transmitting said second current induced from said selected terminal to said common signal line,

said method comprising the steps of:

(a) setting an interconnect characteristic including a film thickness and

permittivity of an insulating layer formed between interconnect layers in a multilayer interconnect structure which is formed in a plurality of layers with the insulating layer sandwiched in between;

(b) obtaining a predetermined capacitance including at least one of said first and second capacitance components by means other than measurement on the basis of said interconnect characteristic set in said step (a);

(c) obtaining said predetermined capacitance by measurement using said capacitance measurement circuit which includes said multilayer interconnect structure within said target capacitance forming section; and

(d) repeatedly performing said step (b) while changing said interconnect characteristic as appropriate so that said predetermined capacitance obtained in said step (b) agrees with said predetermined capacitance obtained in said step (c), and analyzing said interconnect characteristic that is ultimately agreed, as an estimate.

25. A method of analyzing interconnect characteristics using a capacitance measurement circuit,

said capacitance measurement circuit comprising:

first and second terminals;

a current detector detecting a supply current supplied to said first terminal;

a terminal state changer selecting either a first state in which said second terminal is connected to a fixed potential or a second state in which said first and second terminals are short-circuited; and

a target capacitance forming section formed between said first and second terminals and having a measuring target capacitance including first and second capacitance components,

said target capacitance forming section, said first and second terminals, said current detector, and said terminal state changer constituting a capacitance measurement section,

said method comprising the steps of:

(a) setting an interconnect characteristic including a film thickness and permittivity of an insulating layer formed between interconnect layers in a multilayer interconnect structure which is formed in a plurality of layers with the insulating layer sandwiched in between;

(b) obtaining a predetermined capacitance including at least one of said first and second capacitance components by means other than measurement on the basis of said interconnect characteristic set in said step (a);

(c) obtaining said predetermined capacitance by measurement using said capacitance measurement circuit which includes said multilayer interconnect structure within said target capacitance forming section; and

(d) repeatedly performing said step (b) while changing said interconnect characteristic as appropriate so that said predetermined capacitance obtained in said step (b) agrees with said predetermined capacitance obtained in said step (c), and analyzing said interconnect characteristic that is ultimately agreed, as an estimate.

26. A method of analyzing interconnect characteristics using a capacitance measurement circuit,

said capacitance measurement circuit comprising:

a first terminal accompanied by a first capacitance including first and second capacitance components, said first capacitance component including a predetermined number of first capacitance components;

a predetermined number of second terminals;

a first current detector detecting a first current supplied to said first terminal;

a second current detector detecting a second current obtained from a common signal line;

a target capacitance forming section formed between said first terminal and said predetermined number of second terminals so that said first terminal is accompanied by said first capacitance component, said target capacitance forming section having said predetermined number of first capacitance components formed between said first terminal and said predetermined number of second terminals; and

a selector selecting one of said predetermined number of second terminals as a selected terminal in response to an external signal whose bit number is smaller than said predetermined number, and transmitting said second current induced from said selected terminal to said common signal line,

said method comprising the steps of:

(a) setting interconnect characteristics including a film thickness and permittivity of an insulating layer formed between a plurality of interconnect layers and a film thickness of a predetermined one of said plurality of interconnect layers in a multilayer interconnect structure including said plurality of interconnect layers with the insulating layer sandwiched in between;

(b) obtaining a predetermined capacitance accompanying said predetermined interconnect layer and a predetermined resistance that is an interconnect resistance of said predetermined interconnect layer by means other than measurement on the basis of said interconnect characteristics set in said step (a), said predetermined capacitance including said first capacitance component;

(c) obtaining said predetermined capacitance by measurement using said

capacitance measurement circuit which includes said multilayer interconnect structure within said target capacitance forming section;

(d) obtaining said predetermined resistance by measurement using a target resistance forming section provided independently of said target capacitance forming section and including an interconnect resistance pattern structured to have the same target resistance conditions as said predetermined interconnect layer; and

(e) repeatedly performing said step (b) while changing said interconnect characteristics as appropriate so as to satisfy a first condition that said predetermined capacitance obtained in said step (b) agrees with said predetermined capacitance obtained in said step (c) and a second condition that said predetermined resistance obtained in said step (b) agrees with said predetermined resistance obtained in said step (d), and analyzing said interconnect characteristics that are ultimately agreed, as estimates.

27. The method according to claim 26, wherein

said multilayer interconnect structure includes a dummy pattern formed in the same layer as said predetermined interconnect layer and not serving as an interconnect line, and

said interconnect resistance pattern includes a resistance section whose resistance is to be measured, and a mesh interconnect section uninvolved in resistance measurement, said mesh interconnect section being approximately equal in area proportion to said dummy pattern.

28. The method according to claim 26, wherein

said step (e) includes the process of extracting said interconnect characteristics satisfying said first and second conditions at the same time in a collective manner.

29. The method according to claim 26, wherein

said target resistance conditions include an interconnect width, an interconnect length, an interconnect spacing, and an interconnect film thickness.

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